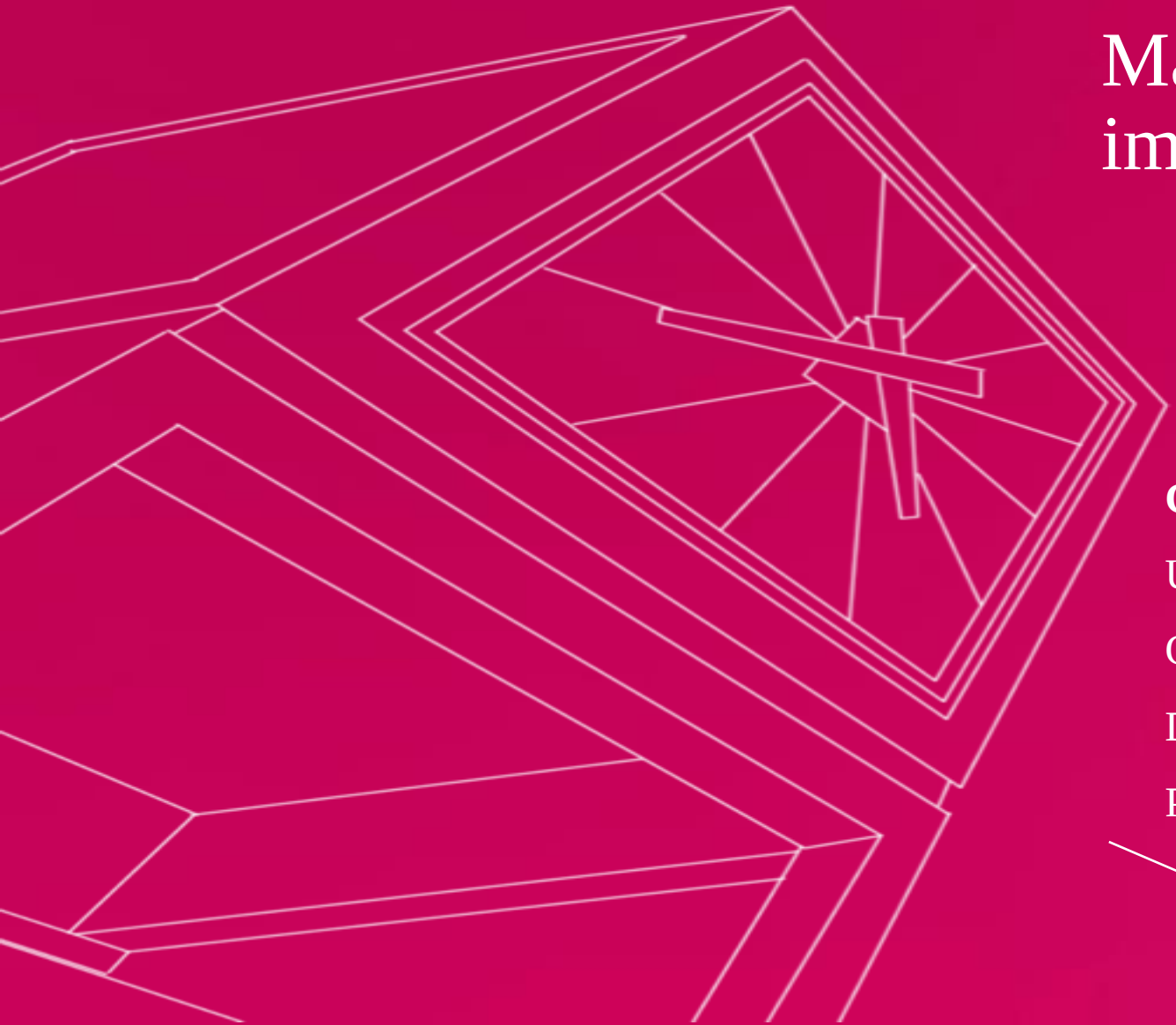


Maximum - speed implementation of ORCA

2019.08.09 Fri

Choi, Geunseok

Undergraduate Student

CAD & SoC Design Lab.

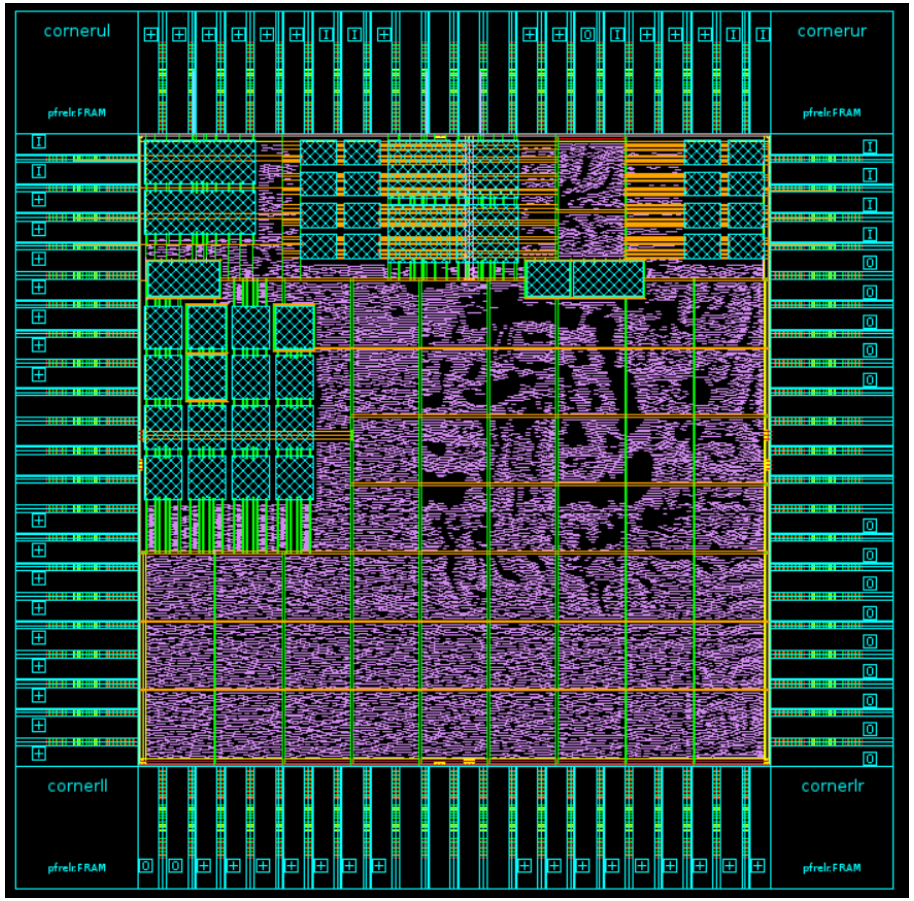
Department of Electrical Engineering

Pohang University of Science and Technology

Focus of Thesis – IC compiler

Maximum-speed implementation of ORCA

✓ Objective : Minmize { Design Area * Minimum Clock Period }



The Conventional

Worst Negative Slack = 1.72 ns

Specified Clock Period = 8 ns

Minimum clock period = 9.72 ns

Design Area = 629209.177001 nm^2

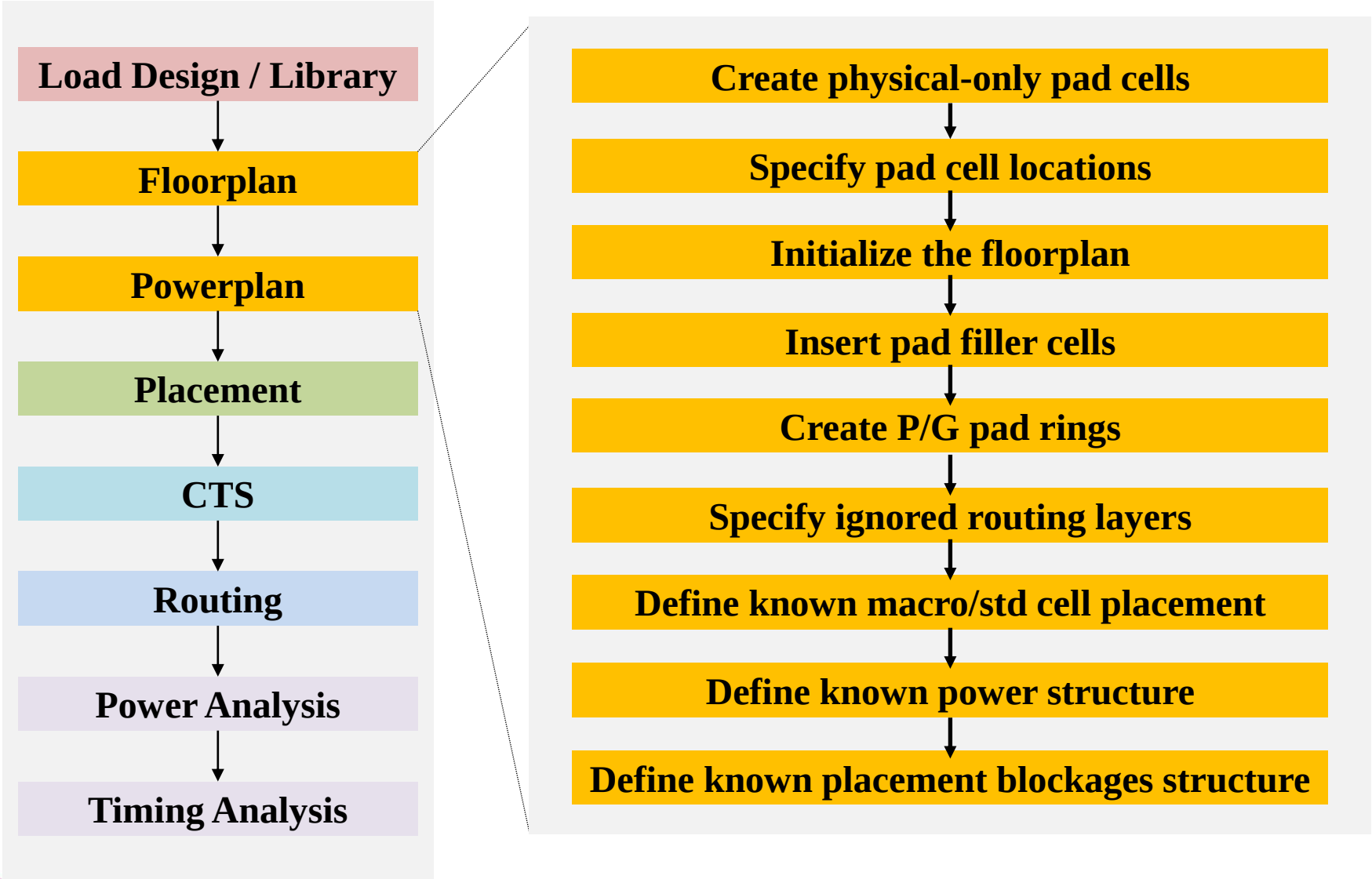
Voltage Supply = 1.32V

Score (Design Area * Minimum Clock Period)

= 6115913.2 # of DRC Error = 10

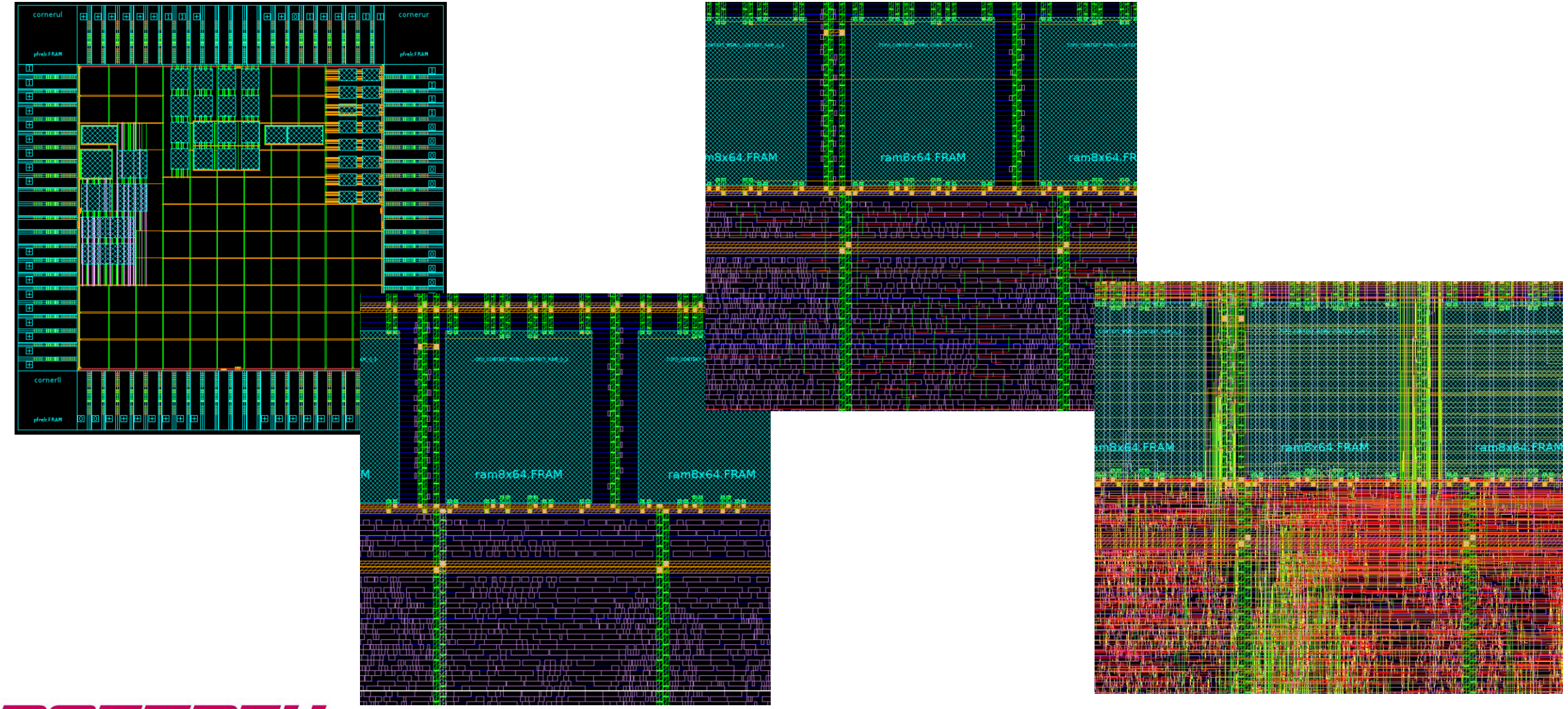
2. Structure

✓ Start Back-End with design(.v), constraints/targets(.sdc), conditions/modes(MMMC), libraries(.lef)



3. Flow – overall

- ✓ Floor plan/Power plan → placement → Clock Tree synthesis → Routing



3. Flow - Data setup

1) Design library/data

```
open_mw_cel -library orca_lib.mw orca_setup

set_tlu_plus_files -max_tluplus $tlup_max -min_tluplus $tlup_min -tech2itf_map $tlup_map
```

2) Design optimization

```
set_host_options -max_cores 8

set_max_area 0
```

3) Check over-constraint

```
Path Group: INPUTS
Path Type: max

Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock SDRAM_CLK (fall edge)                             3.75       3.75
clock network delay (ideal)                             0.00       3.75
input external delay                                    0.80       4.55 r
sd_DQ[0] (inout)                                        0.00 z     4.55 r
sdram_DQ_iopad_0/PAD (pc3b05)                           0.00 z     4.55 r
sdram_DQ_iopad_0/CIN (pc3b05)                           0.93 z     5.48 r
I_ORCA_TOP/sd_DQ_in[0] (ORCA_TOP)                       0.00 z     5.48 r
I_ORCA_TOP/I_SDRAM_TOP/sd_DQ_in[0] (SDRAM_TOP)          0.00 z     5.48 r
I_ORCA_TOP/I_SDRAM_TOP/I_SDRAM_IF/sd_DQ_in[0] (SDRAM_IF)
                                                        0.00 z     5.48 r
I_ORCA_TOP/I_SDRAM_TOP/I_SDRAM_IF/DQ_in_0_reg_0_/D (sdnrq1)
                                                        0.00 z     5.48 r
data arrival time                                                  5.48

clock SDRAM_CLK (rise edge)                             7.50       7.50
clock network delay (ideal)                             0.00       7.50
clock uncertainty                                      -0.10       7.40
I_ORCA_TOP/I_SDRAM_TOP/I_SDRAM_IF/DQ_in_0_reg_0_/CP (sdnrq1)
                                                        0.00       7.40 r
library setup time                                     -0.22       7.18
data required time                                                 7.18
-----------------------------------------------------------------------------
data required time                                                 7.18
data arrival time                                                 -5.48
-----------------------------------------------------------------------------
slack (MET)                                                        1.70
```

```
### zero-interconnect timing checking

set_zero_interconnect_delay_mode true

report_constraint -all

report_timing

set_zero_interconnect_delay_mode false
```

3. Flow – Floorplan/Powerplan

1) Create P/G pads and conncet

```
source -echo scripts/pad_cell_cons.tcl

create_floorplan -core_utilization 0.5 -left_io2core 10.0 -bottom_io2core 10.0 -right_io2core 10.0 -top_io2core 10.0

insert_pad_filler -cell "pfeed10000 pfeed05000 pfeed02000 pfeed01000 pfeed00500 pfeed00200 pfeed00100 pfeed00050 pfeed00010 pfeed00005"

source -echo scripts/connect_pg.tcl

create_pad_rings

save_mw_cel -as floorplan_init
```

2) Macro cell placement

```
source -echo scripts/preplace_macros.tcl

set_fp_placement_strategy -auto_grouping high -macros_on_edge on -sliver_size 10 -virtual_IPO on

set_fp_macro_options -legal_orientation {W E} [get_cells I_ORCA_TOP/I_PCI_TOP/I_PCI_WRITE_FIFO/PCI_FIFO_RAM_*]

create_fp_placement -timing_driven -no_hierarchy_gravity

set_keepout_margin -type hard -all_macros -outer {10 10 10 10}

create_fp_placement -timing_driven -no_hierarchy_gravity

set_dont_touch_placement [all_macro_cells]
```

3. Flow – Floorplan/Powerplan

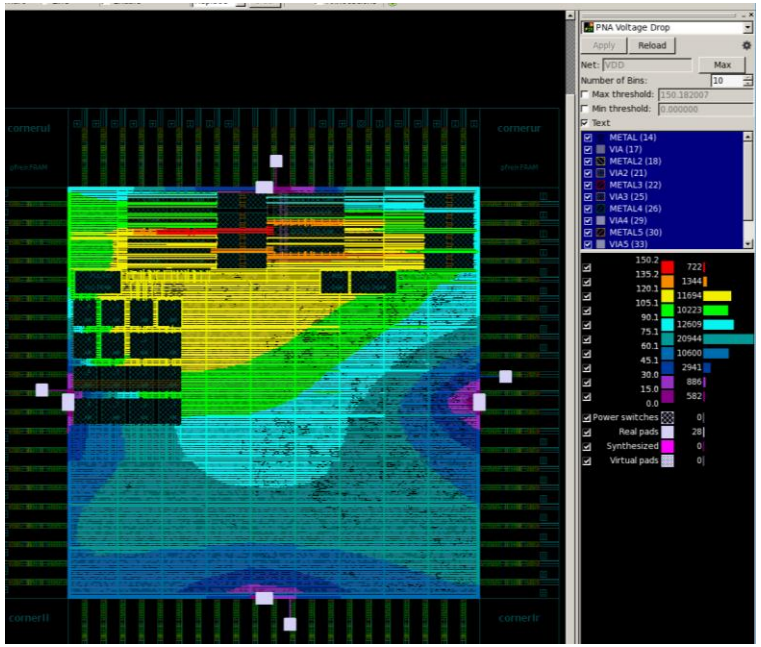
1) Check congestion – GRCs is less than 0.1%

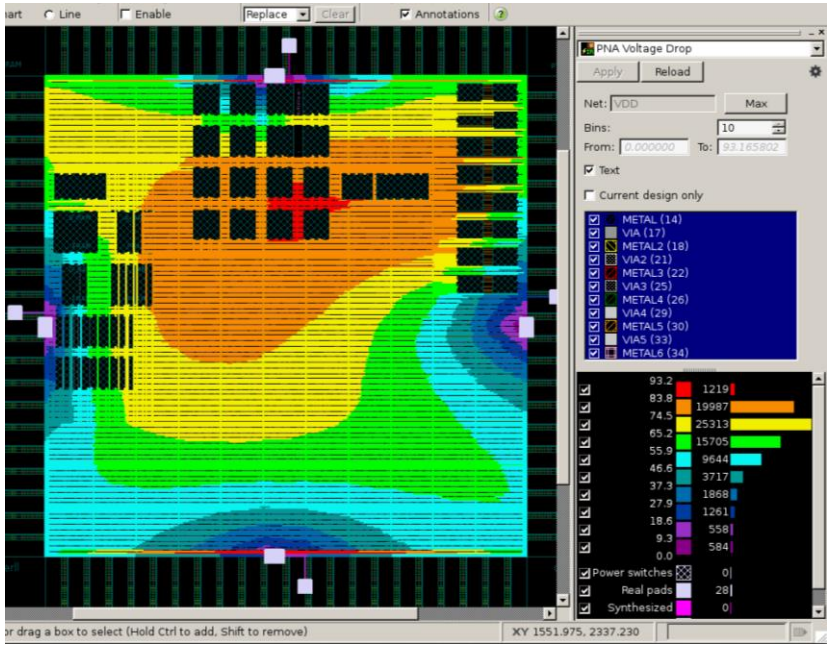
```
phase1. Routing result:
phase1. Both Dirs: Overflow =   171 Max = 2 GRCs =   316  0.03%)
phase1. H routing: Overflow =    73 Max = 1 (GRCs =  28) GRCs =   232 (0.05%)
phase1. V routing: Overflow =    98 Max = 2 (GRCs =  16) GRCs =    84 (0.02%)
phase1. METAL      Overflow =    32 Max = 0 (GRCs = 180) GRCs =   180 (0.04%)
phase1. METAL2     Overflow =    98 Max = 2 (GRCs =  16) GRCs =    84 (0.02%)
phase1. METAL3     Overflow =    40 Max = 1 (GRCs =  28) GRCs =    52 (0.01%)
phase1. METAL4     Overflow =     0 Max = 0 (GRCs =   0) GRCs =     0 (0.00%)
phase1. METAL5     Overflow =     0 Max = 0 (GRCs =   0) GRCs =     0 (0.00%)
phase1. METAL6     Overflow =     0 Max = 0 (GRCs =   0) GRCs =     0 (0.00%)
```

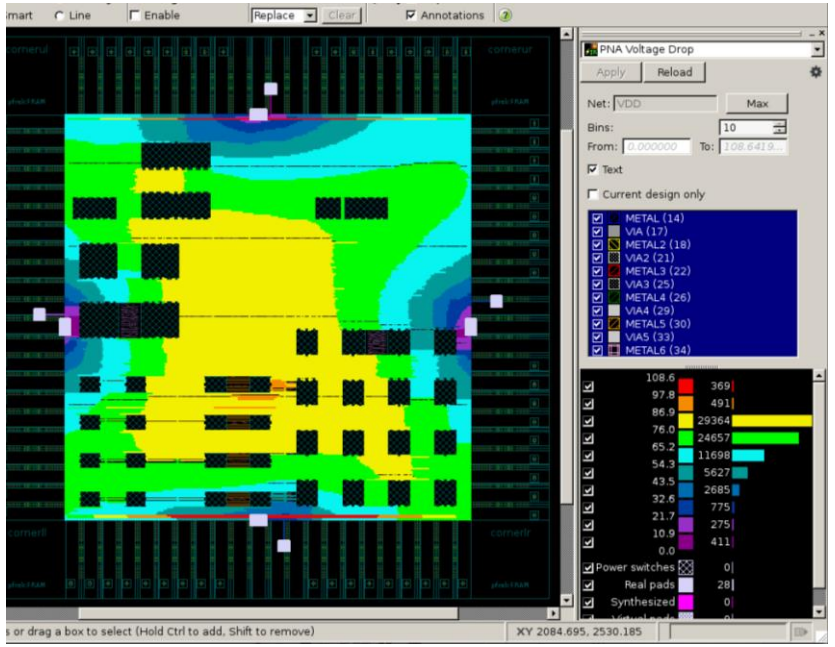
```
create_fp_placement -timing_driven -no_hierarchy_gravity

route_zrt_global -congestion_map_only true -exploration true
```

2) Check IR-drop – left : conventional / right : optimized

```
analyze_fp_rail -nets {VDD VSS} -voltage_supply 1.32 -power_budget 350 -pad_masters { pv0i pvdi }
```







3. Flow – Placement

1) Placement

```
create_placement_blockage -coordinate {{345.415 345.145} {2141.135 367.190}} -name placement_blockage_3 -type hard

place_opt -area_recovery -effort high -power -congestion
```

2) Congestion analysis

```
route_zrt_global -cong true -exploration true
```

3) Timing analysis

```
report_constraint -max_delay -all_violators -scenario [all_active_scenarios]
```

4) optimization

```
psynopt -area_recovery -power -congestion
```

```
****************************************
Report : constraint
        -all_violators
        -max_delay
Design : ORCA
Version: O-2018.06
Date   : Thu Aug  8 15:33:20 2019
****************************************

        Parasitic source     : LPE
        Parasitic mode       : RealRVirtualC
        Extraction mode      : MIN_MAX
        Extraction derating  : 125/125/125
This design has no violated constraints.
```

```
phase1. Routing result:
phase1. Both Dirs: Overflow =    26 Max = 1 GRCs =   128 (0.01%)
phase1. H routing: Overflow =    26 Max = 1 (GRCs =  12) GRCs =   128 (0.03%)
phase1. V routing: Overflow =     0 Max = 0 (GRCs =   0) GRCs =     0 (0.00%)
phase1. METAL      Overflow =    13 Max = 0 (GRCs = 104) GRCs =   104 (0.02%)
phase1. METAL2     Overflow =     0 Max = 0 (GRCs =   0) GRCs =     0 (0.00%)
phase1. METAL3     Overflow =     4 Max = 1 (GRCs =   4) GRCs =    12 (0.00%)
phase1. METAL4     Overflow =     0 Max = 0 (GRCs =   0) GRCs =     0 (0.00%)
phase1. METAL5     Overflow =     8 Max = 1 (GRCs =   8) GRCs =    12 (0.00%)
phase1. METAL6     Overflow =     0 Max = 0 (GRCs =   0) GRCs =     0 (0.00%)
```

3. Algorithm – CTS

1) CTS design setting

```
remove_ideal_network [all_fanout -flat -clock_tree]

set_delay_calculation_options -routed_clock arnoldi

set_clock_tree_options -target_skew 0.2

set_clock_uncertainty 0.2 [all_clocks]

set_clock_tree_references -references {bufbd1 bufbd2 bufbd4 bufbd7 bufbdf}

define_routing_rule  CLOCK_DOUBLE_SPACING -spacings {METAL3 0.42 METAL4 0.63 METAL5 0.82}
```

2) CTS implement

```
clock_opt -only_cts -no_clock_route -inter_clock_balance

extract_rc

clock_opt -only_psyn -no_clock_route -power -area_recovery
```

1) Clock tree skew

```
======================== Clock Tree Summary ========================
Clock                 Sinks     CTBuffers ClkCells  Skew      LongestPath TotalDRC
------------------------------------------------------------------------------------
pclk                  623       28        32        0.3525    1.4725      0
sdr_clk               2138      97        102       0.1851    1.5182      0
PCI_CLK               621       21        23        0.0349    0.5452      0
SDRAM_CLK             2137      90        93        0.4598    0.8920      0
SD_DDR_CLK            0         0         0         0.0000    0.0000      0
Global Settings for clock trees
------------------------------
```

3. Algorithm – CTS

2) Clock tree skew

```
Path Group: SYS_CLK
Path Type: max

Point                                                    Incr       Path
-----------------------------------------------------------------------
clock SYS_CLK (rise edge)                                0.00       0.00
clock network delay (propagated)                         1.85       1.85
I_ORCA_TOP/I_BLENDER_3/s3_op1_reg_0_/CP (sdnrq1)         0.00       1.85 r
I_ORCA_TOP/I_BLENDER_3/s3_op1_reg_0_/Q (sdnrq1)          0.39       2.24 r
I_ORCA_TOP/I_BLENDER_3/sub_171/B[0] (BLENDER_5_DW01_sub_0)
                                                         0.00       2.24 r
                                    .
                                    .
                                    .

clock SYS_CLK (rise edge)                                8.00       8.00
clock network delay (propagated)                         1.75       9.75
clock uncertainty                                       -0.20       9.55
I_ORCA_TOP/I_BLENDER_3/s4_op2_reg_30_/CP (sdnrq1)        0.00       9.55 r
library setup time                                      -0.17       9.39
data required time                                                  9.39
-----------------------------------------------------------------------
data required time                                                  9.39
data arrival time                                                  -9.14
-----------------------------------------------------------------------
slack (MET)                                                         0.25
```

3) Clock tree slack & violoation

```
Timing Path Group 'pclk'
----------------------------------
Levels of Logic:                0.00
Critical Path Length:           0.35
Critical Path Slack:            7.21
Critical Path Clk Period:      15.00
Total Negative Slack:           0.00
No. of Violating Paths:         0.00
Worst Hold Violation:           0.00
Total Hold Violation:           0.00
No. of Hold Violations:         0.00
----------------------------------

Timing Path Group 'sdr_clk'
----------------------------------
Levels of Logic:                1.00
Critical Path Length:           0.48
Critical Path Slack:            6.50
Critical Path Clk Period:       7.50
Total Negative Slack:           0.00
No. of Violating Paths:         0.00
Worst Hold Violation:           0.00
Total Hold Violation:           0.00
No. of Hold Violations:         0.00
----------------------------------
```

3. Flow – Routing

1) Route option setting

```
set_delay_calculation_options -postroute arnoldi

set_route_zrt_common_options -post_detail_route_redundant_via_insertion medium

set_route_zrt_global_options -timing_driven true -crosstalk_driven true
```

2) Inial route and optimize

```
route_zrt_group -all_clock_nets -reuse_existing_global_route true

route_opt -initial_route_only

route_opt -skip_initial_route -effort high -xtalk_reduction -power
```

3) Vertification – DRCs & LVS

```
Verify Summary:

Total number of nets = 54173, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                 0 ports without pins of 0 cells connected to 0 nets
                                 0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 4
Total number of antenna violations = no antenna rules defined
Total number of voltage-area violations = no voltage-areas defined
Total number of tie to rail violations = not checked
Total number of tie to rail directly violations = not checked
```

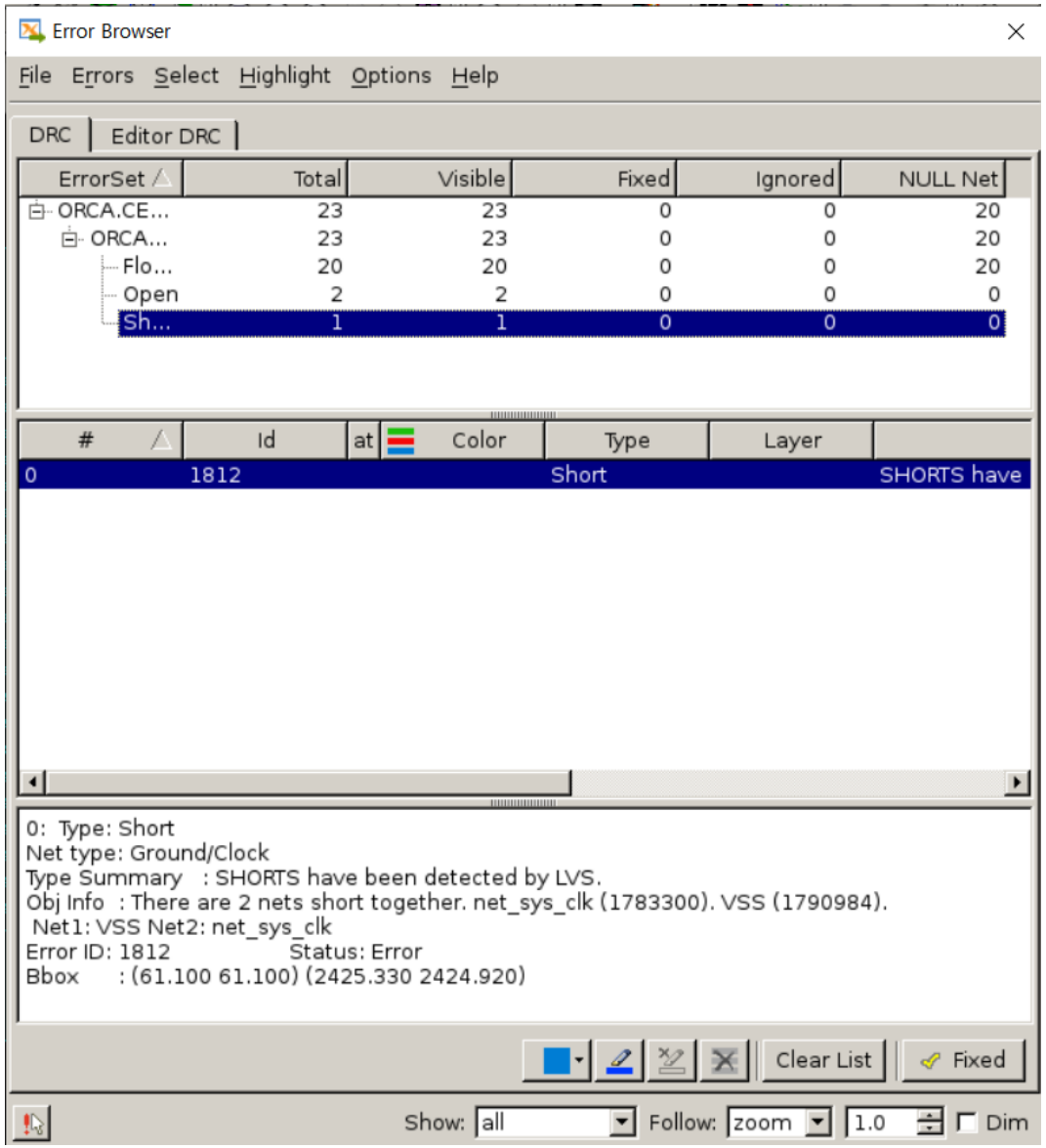
```
icc_shell> verify_pg_nets
Cell orca_setup.err existed already. Delete it ...
Using [4 x 4] Fat Wire Table for METAL
Using [4 x 4] Fat Wire Table for METAL2
Using [4 x 4] Fat Wire Table for METAL3
Using [4 x 4] Fat Wire Table for METAL4
Using [3 x 3] Fat Wire Table for METAL5
Using [3 x 3] Fat Wire Table for METAL6
Checking [VSSQ]:
        There are no floating shapes
        All the pins are connected.
        No errors are found.
Checking [VDDQ]:
        There are no floating shapes
        All the pins are connected.
        No errors are found.
Checking [VSSO]:
        There are no floating shapes
        All the pins are connected.
        No errors are found.
Checking [VDDO]:
        There are no floating shapes
        All the pins are connected.
        No errors are found.
Checking [VSS]:
        There are no floating shapes
        ERROR: There are 222 floating pins
Checking [VDD]:
        There are no floating shapes
        ERROR: There are 162 floating pins
Checked 6 nets, 2 have Errors
```

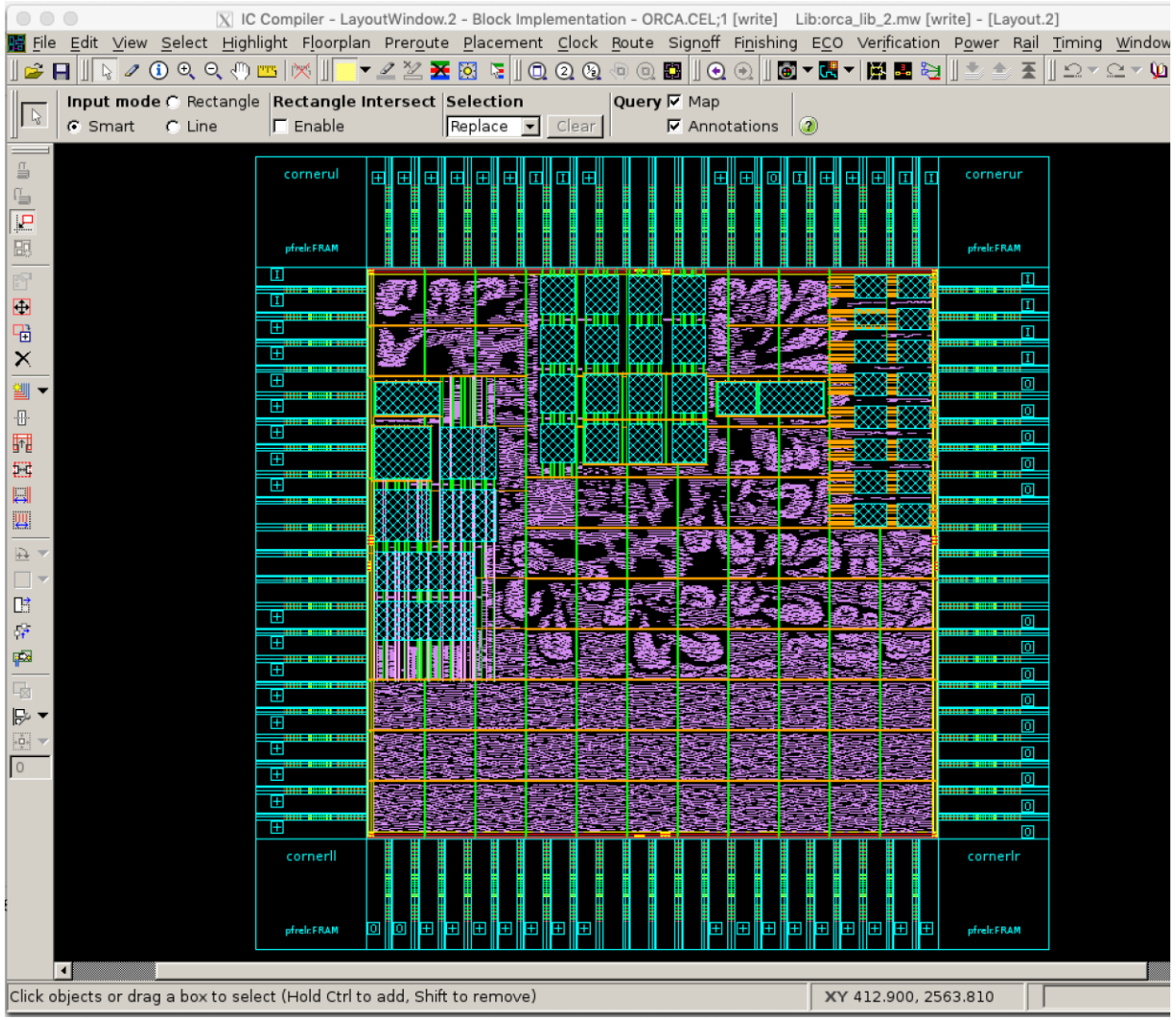
4. Result

- ✓ Minimum clock period are reduced by 58% compared with the conventional
- ✓ Score is reduced by 58% compared with the conventional
- ✓ DRC is reduce by 40% compared with the conventional
- ✓ Area is almost same with the conventional

	sys_clk	WNS	minimum clk	Area	Score	Improvement	DRC
Conventional	8.00	1.72	9.72	629209.18	6115913.20	-	10.00
EE753(2017) S1	4.00	0.78	4.78	659977.44	3154692.16	48.42	7.00
EE753(2017) S2	6.00	0.14	6.14	645134.54	3961126.08	35.23	6.00
mine	4.00	0.00	4.00	629135.91	2516543.66	58.85	4.00

4. Result


Error Browser
File Errors Select Highlight Options Help
DRC Editor DRC
ErrorSet Total Visible Fixed Ignored NULL Net
ORCA.CE... 23 23 0 0 20
ORCA... 23 23 0 0 20
Flo... 20 20 0 0 20
Open 2 2 0 0 0
Sh... 1 1 0 0 0
Id at Color Type Layer
0 1812 Short SHORTS have
0: Type: Short
Net type: Ground/Clock
Type Summary : SHORTS have been detected by LVS.
Obj Info : There are 2 nets short together. net_sys_clk (1783300). VSS (1790984).
Net1: VSS Net2: net_sys_clk
Error ID: 1812 Status: Error
Bbox : (61.100 61.100) (2425.330 2424.920)
Clear List
Fixed
Show: all
Follow: zoom
1.0
Dim


IC Compiler - LayoutWindow.2 - Block Implementation - ORCA.CEL;1 [write] Lib:orca_lib_2.mw [write] - [Layout.2]
File Edit View Select Highlight Floorplan Preroute Placement Clock Route Signoff Finishing ECO Verification Power Rail Timing Window
Input mode Rectangle Smart Line
Rectangle Intersect Enable
Selection Replace Clear
Query Map Annotations
cornerul
cornerur
cornerll
cornerlr
pfrelcFRAM
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
XY 412.900, 2563.810